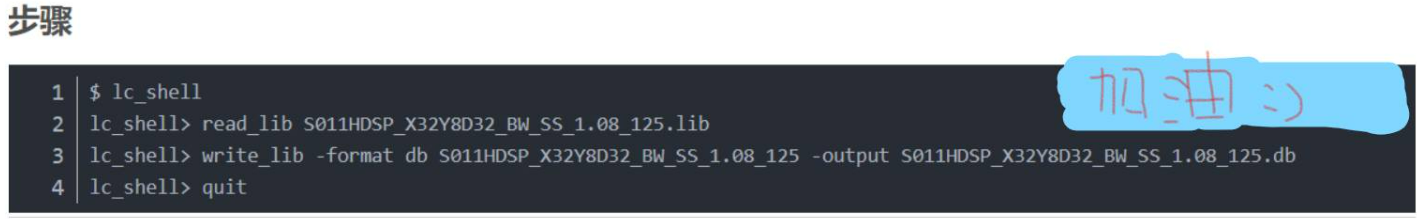
**Convert the .lib to .db for synthesis**



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**If you are not familiar with verilog, we recommend a website for learning verilog**

* https://hdlbits.01xz.net/wiki/Main\_Page

--> Answer: <https://blog.csdn.net/wangkai_2019/article/details/106664283>

**Before run the synthesis, you need to**

1. **Generate the .db file**
2. **Create a file “Report”**